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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/649,808	08/28/2003	Klaas Bult	1875.0510002	5778

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EXAMINER	
LAM, TUAN THIEU	
ART UNIT	PAPER NUMBER
2816	

SHORTENED STATUTORY PERIOD OF RESPONSE	NOTIFICATION DATE	DELIVERY MODE
3 MONTHS	01/24/2007	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Notice of this Office communication was sent electronically on the above-indicated "Notification Date" and has a shortened statutory period for reply of 3 MONTHS from 01/24/2007.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

fadkt@skgf.com

Office Action Summary	Application No.	Applicant(s)	
	10/649,808	BULT ET AL.	
	Examiner	Art Unit	
	Tuan T. Lam	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 November 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6 and 21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6 and 21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01 June 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

This is a response to the amendment filed 11/17/2006. Claims 1-6 and 21 are pending and are under examination.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-2 and 4-6 are rejected under 35 U.S.C. 102(b) as being anticipated by Zerbe (USP 5,977,798).

Figure 3 of Zerbe shows a latch circuit comprising a bistable pair of transistors (112, 113) connected between a reset switch (114) and a first supply voltage (ground), and having a first port (200) for receiving a first current signal (current flows along the transistor 100) and producing a first output voltage, and a second port (201) for receiving a second current signal (current flows along the transistor 101) and producing a second output voltage, and a vertical latch (108, 100, 101, 109, 110, 111) having a first transistor (110) and a second transistor (100) and connected between said first supply voltage and a second supply voltage (Vdd and ground), said first transistor (110) connected to said first port (200), when said first transistor (110) is turned on, a current flows from said second supply voltage (Vdd) through said first transistor to said first port, said first transistor is first type (PMOS) and said second transistor (NMOS) is a second type different from the first type, wherein said bistable pair of transistors are connected directly to said first supply voltage as called for in claim 1.

Regarding claim 2, said transistor is a MOSFET.

Regarding claim 4, the vertical latch is capable of decreasing the time necessary for said first port to reach a steady stage voltage in response to said first current signal received.

Regarding claim 5, figure 3 shows a vertical latch reset switch 104 connected to the vertical latch.

Regarding claim 6, figure 3 shows a second vertical latch (106, 107) connected between said first supply voltage and second supply voltage and said second port.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Zerbe (USP 5,977,798) in view of Lin et al. (US 20010048141).

Figure 3 of Zerbe shows a latch circuit comprising a bistable pair of transistors (112, 113) connected between a reset switch (114) and a first supply voltage (ground), and having a first port (200) for receiving a first current signal (current flows along the transistor 100) and producing a first output voltage, and a second port (201) for receiving a second current signal (current flows along the transistor 101) and producing a second output voltage, and a vertical latch (108, 100, 101, 109, 110, 111) having a first transistor (110) and a second transistor (100) and connected between said first supply voltage and a second supply voltage (Vdd and ground),

said first transistor (110) connected to said first port (200), when said first transistor (110) is turned on, a current flows from said second supply voltage (Vdd) through said first transistor to said first port, said first transistor is first type (PMOS) and said second transistor (NMOS) is a second type different from the first type, wherein said bistable pair of transistors are connected directly to said first supply voltage.

Zerbe reference shows the reset switch as an electronic switch (MOS transistor) instead of a microelectromechanical switch as called for in claim 3.

Paragraph 0002 of Lin et al. teaches that microelectromechanical switch provides minimal insertion loss and capable of handling power. Therefore, it would have been obvious to person skilled in the art at the time the invention was made to replace Zerbe's transistor reset switch with a microelectromechanical switch for the purpose of maintaining minimal insertion loss and capable of handling power.

5. Claim 21 is rejected under 35 U.S.C. 103(a) as being unpatentable over Zerbe (USP 5,977,798) in view of Lin et al. (US 20010048141).

Figure 3 of Zerbe reference shows a latch circuit comprising a first transistor (112) coupled between a first port (200) and a supply voltage (ground), second transistor (113) coupled between a second port (201) and said supply voltage, a reset switch (114) coupled between said first port and said second port, wherein said first transistor and said second transistor are configured in a bistable pair, said first port (200) to receive a first current signal (current flows from transistor 100 to the first port) to produce a first output voltage, and said second port (201) is configured to receive a second current signal (current signal flows from transistor 101) and to produce a second output voltage.

Zerbe reference shows the reset switch as an electronic switch (MOS transistor) instead of a microelectromechanical switch as called for in claim 21.

Paragraph 0002 of Lin et al. teaches that microelectromechanical switch provides minimal insertion loss and capable of handling power. Therefore, it would have been obvious to person skilled in the art at the time the invention was made to replace Zerbe's transistor reset switch with a microelectromechanical switch for the purpose of maintaining minimal insertion loss and capable of handling power.

Conclusion

6. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tuan T. Lam whose telephone number is 571-272-1744. The examiner can normally be reached on Monday to Friday (7:30 am to 6:00pm).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, TIMOTHY P. CALLAHAN can be reached on 571-272-1740. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Tuan T Lam
Primary Examiner
Art Unit 2816

1/15/2007